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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/725,853	12/01/2003	Donald R. DeSota	BEA920020011US1	3245

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LAW OFFICES OF MICHAEL DRYJA
704 228TH AVE NE
#694
SAMMAMISH, WA 98074

EXAMINER	
KROFCHECK, MICHAEL C	

ART UNIT	PAPER NUMBER
2186	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/725,853	DESOTA ET AL.	
	Examiner	Art Unit	
	Michael Krofcheck	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,7-14,16-18 and 20* is/are rejected.

7)☒ Claim(s) *6,15 and 19* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to application 10/725,853 filed on 12/01/2003.

2. Claims 1-20 have been submitted for examination.

3. Claims 1-20 have been examined.

Specification

4. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

5. The abstract of the disclosure is objected to because the second line contains the phrase, "...a coherency controller of a node is ***disclosed***". Correction is required. See MPEP § 608.01(b).

Claim Objections

6. Claims 4-7 are objected to because of the following informalities:

a. With respect to claim 4, the lack of punctuation (specifically commas) throughout the claim makes it difficult to read and understand. The examiner requests that the applicant modify the punctuation in the two phrases beginning with "one or more of not being..." in line 2 and 4 in the same manner as the phrase is punctuated in claim 1.

b. With respect to claim 5, as in the above claim 4, The examiner requests that the applicant modify the punctuation in the phrase beginning with "one or more of not being..." in line 2 in the same manner as the phrase is punctuated in claim 1.

c. Claims 6-7 are objected to because of their dependency.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. Claims 1-5, 8-9, and 18 are rejected under 35 U.S.C. 102(b) as being anticipated by Luick et al., U.S. Patent 6,088,769 (hereinafter Luick).

9. With respect to claim 1, Luick teaches of a method for performance by a coherency controller (fig. 1, items 109, 113) of a node, comprising: receiving a

transaction relating to a line of local memory of the node (figs. 1, 3, item 301; column 6, lines 49-56); and

in response to determining locally within the controller that the line of the local memory is one or more of not being cached by any other node, and has not been modified by any other node (figs. 1, 3, items 303, 305, 309; column 6, line 56-column 7, line 5; column 5, lines 39-44; the LCT contains a bit associated with each cache line of data within the memory. That bit indicates if the current locally stored data at that address is the most current copy of that data (has the data been modified or not). The cache controller checks the LCU to determine if the locally stored data is the most current data),

processing the transaction by the coherency controller without accessing information regarding the line of local memory in a tag directory associated with the local memory (fig. 3, item 307, 311; column 6, line 63-column 7, line 9; if the most current copy of the data (not modified copy) is in the local cache the data read request is serviced. If the most current copy of the data is in the local memory, then the data is copied to the cache and then accessed by the processor. In these steps, the GCU (tag directory) is not consulted).

10. With respect to claim 2, Luick teaches of all the limitations of the parent claim as discussed supra. Luick also teaches of otherwise, processing the transaction by the coherency controller such that the coherency controller accesses information regarding the line of local memory in the tag directory (fig 3, items 313; column 7, lines 10-41;

where the controller sends a request to the GCU (tag directory) to process the initial request).

11. With respect to claim 3, Luick teaches of all the limitations of the parent claim as discussed supra. Luick also teaches of wherein accessing information regarding the line of local memory in the tag directory results in slower processing of the transaction than if information regarding the line of local memory in the tag directory were not accessed (figs. 1, 3; When processing the request without the GCU, the LCU is checked and then the data is read out from its location (request processed). When accessing the GCU to process the request, the LCU is checked and the additional steps of sending requests/data to the GCU, from the GCU to the other node, and back to the requesting node are undertaken before the data can be read out. Therefore, it must be slower to process a request via the GCU).

12. With respect to claim 4, wherein determining locally within the controller that the line of the local memory is one or more of not being cached by any other node and has not been modified by any other node comprises examining a table within the coherency controller to determine that the line of the local memory is one or more of not being cached by any other node and has not been modified by any other node (figs. 1-3; column 4, lines 23-26; line 54-column 5, line 13; column 6, line 56-column 7, line 14; The cache controller accesses the LCU processor which check the LCU table to determine if the requested data stored in the node has been modified by another node).

13. With respect to claim 5, Luick teaches of all the limitations of the parent claim as discussed supra. Luick also teaches of wherein looking up the line of local memory

within the table of the coherency controller to determine that the line of the local memory is one or more of not being cached by any other node and has not been modified by any other node comprises referencing an entry within the table of the coherency controller corresponding to a section of the local memory including the line of local memory (fig. 2; column 4, lines 23-53; The LCT contains one entry associated with each cache line stored within the memory. The address of the portion of memory is used as an index to the entry in the LCT).

14. With respect to claim 8, Luick teaches of all the limitations of the parent claim as discussed supra. Luick also teaches of wherein processing the transaction by the coherency controller comprises processing the transaction by a coherency processor of the coherency controller (column 7, lines 2-9; where the cache controller makes the data available to the processor. As the controller directs the processing of the request, there must be a processor within the controller that commands the various parts of the controller, thus processing the transaction).

15. With respect to claim 9, Luick teaches of all the limitations of the parent claim as discussed supra. Luick also teaches of wherein processing the transaction without accessing information regarding the line of memory in the tag directory results in faster processing of the transaction than if information regarding the line of memory in the tag directory were accessed (figs. 1, 3; When processing the request without the GCU, the LCU is checked and then the data is read out from its location (request processed). When accessing the GCU to process the request, the LCU is checked and the additional steps of sending requests/data to the GCU, from the GCU to the other node,

and back to the requesting node are undertaken before the data can be read out. Therefore, it must be significantly faster to process a request without accessing the GCU).

16. With respect to claim 18, Luick teaches of a coherency controller (fig. 1; items 109, 113) for a node of a system to process transactions relative to at least a portion of memory of the node, comprising: a coherency processor within which transactions are converted into performable actions to effect the transactions relative to at least the portion of the memory of the node (figs. 1, 3; column 6, line 56-column 7, line 13; where the cache controller (coherency controller) determines the location of the most current copy of the data, steps 303, 305, 309. If the most current copy is local, the cache controller makes the data accessible to the processor and if it is not local, the cache controller sends a request to the GCU to locate it. As the cache controller performs these actions and must include processor to control the actions, the requests are converted into actions by the processor); and

a local region table storing access information regarding at least the portion of the memory of the node by other nodes of the system so that the coherency controller may be able to convert the transactions within the pipeline without accessing tag directory information associated with the memory of the node (fig. 1; item 121; column 5, line 54-column 6, line 13; where the LCT (local region table) indicates whether or not another node has read out each cache line).

Claim Rejections - 35 USC § 103

17. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

18. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

19. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

20. Claims 10-14 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Luick.

21. With respect to claim 10, Luick teaches of a node of a multi-node system comprising: one or more processors (fig. 1; item 103; column 4, lines 1-2);

local memory for the processor(s) (fig. 1; item 105; column 4, lines 1-2);

at least one memory controller to process memory operations relative to the local memory (fig. 1; item 113;);

at least one coherency controller to process transactions relative to the local memory (fig. 1; items 113 and 109; column 4, line 3; column 5, lines 8-13); and

a local region table within each coherency controller storing access information regarding the local memory by other nodes of the multi-node system so that the coherency controller is able to process the transactions relative to the local memory without accessing tag directory information associated with the local memory (fig. 1; item 121; column 4, line 54-column 5, line 13).

Luick fails to teach of using a RAM as the local memory. However, using RAMs as a local memory is conventional and well known in the art.

It would have been obvious to one of ordinary skill in the art at the time of the invention to implement the local memory in each node of Luick in a RAM as they are the most common type of computer memory and provide faster access times than ROMs.

22. With respect to claim 11, Luick teaches of the limitations of the parent claim as discussed supra. Luick also teaches of a coherency processor within the coherency controller within which the transactions are processed (fig. 1; item 119; column 4; lines 23-24).

23. With respect to claim 12, Luick teaches of the limitations of the parent claim as discussed supra. Luick also teaches of a tag directory within which the tag directory information is stored (figs. 1, 2; item 123; column 5, lines 15-35; where the GCU (tag directory) contains a GCU table (tag directory information)).

24. With respect to claim 13, Luick teaches of the limitations of the parent claim as discussed supra. Luick also teaches of a tag bus connecting the coherency controller to the tag directory (fig. 1; column 5; lines 14-18; where the GCU is connected by a bus

(tag bus) to the interconnect bus which connects the GCU to the cache controller (part of the coherency controller) via a bus interface).

25. With respect to claim 14, Luick teaches of the limitations of the parent claim as discussed supra. Luick also teaches of wherein the coherency controller accesses the local regional table with less latency than the coherency controller accesses the tag directory (fig. 1; column 1, lines 27-46; The LCU table is located in the LCU as a part of the controller. The GCU table is located in the GCU which is connected to the controller via multiple bus interfaces, and an interconnect bus. The latency of the controller accessing the LCU table must be lower than the latency of the controller accessing the GCU table since the LCU is a part of the controller and the GCU is at a remote location. It is analogous to the latency associated with accessing a cache memory compared to a standard memory (RAM)).

26. With respect to claim 16, Luick teaches of the limitations of the parent claim as discussed supra. Luick also teaches of wherein the local region table has a plurality of flags corresponding to sections of the local memory (fig. 2; column 5, lines 36-44; where the LCT contains a single bit (flag) associated with each cache line),

each flag indicating whether another node has checked out lines within the section of the local memory (fig. 2; column 5, lines 36-44; where the LCT contains a single bit (flag) associated with each cache line that signifies if the data was read (checked out) by another node).

Luick fails to teach of using a RAM as the local memory. However, using RAMs as a local memory is conventional and well known in the art.

27. Claims 17 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Luick as applied to claims 10 and 18 respectively, and further in view of Glasco, U.S. Patent 6,950,913 (hereinafter Glasco).

28. With respect to claim 17 and 20, Luick teaches of the limitations of the parent claim as discussed supra. Luick fails to explicitly teach of wherein the coherency controller comprises an application specific integrated circuit (ASIC). However, Glasco teaches of wherein a coherency controller comprises an application specific integrated circuit (ASIC) (fig. 2; column 8, lines 35-42; where the coherence controller is an ASIC).

Luick and Glasco are analogous arts as they are both in the same field of endeavor, multiprocessor systems. It would have been obvious to one of ordinary skill in the art having the teachings of Luick and Glasco at the time of the invention to implement the cache controller and LCU of Luick as an ASIC as the coherence controller in Glasco is. The motivation for this would have been to improve performance of the controller as the ASIC would be specifically made to do the job thus not having the overhead of fetching and interpreting stored instructions as a general purpose processor would.

29. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Luick as applied to claim 5, and further in view of Liberty U.S. Patent 6,275,900 (hereinafter Liberty).

30. With respect to claim 7, Luick teaches of the limitations of the parent claim as discussed supra. Luick teaches of wherein referencing the entry within the table of the coherency controller corresponding to a section of the local memory including the line of

local memory comprises determining from a flag within the entry in the table whether another node has checked out lines within the section of local memory (fig. 2; column 5, lines 36-44; where the LCT contains a single bit (flag) associated with each cache line that signifies if the data was read (checked out) by another node).

Luick fails to explicitly teach of an operating system (OS) checking out lines within the section of local memory. However Liberty teaches of independent operating systems running on each node (column 9, lines 32-40).

Luick and Liberty are analogous arts as they are both in the same field of endeavor, multiprocessor systems. It would have been obvious to one of ordinary skill in the art having the teachings of Luick and Liberty at the time of the invention to incorporate the independent operating systems on each node in Liberty in each node of Luick. The motivation for this would have been to allow for each node to operate independently.

The operating system of a node controls the processes and actions performed by each node and its components. If another node reads out (checks out) a memory line in the memory; the operating system running that node is controlling the processes that requested and read out the data. Thus, the operating system has read out those lines.

Allowable Subject Matter

31. Claims 6, 15, and 19 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

32. The following is a statement of reasons for the indication of allowable subject matter:

a. With respect to claims 6, 15, and 19, the prior art Luick and Michael et al. U.S. Patent Application Publication 2001/0034816 teach of a local region table with an entry corresponding to sections of the local memory, where the entry contains a bit that signifies if the memory line has been modified by another node (Luick, column 5, lines 37-44). Since the bit is set when the cache line is modified, it could be interpreted that the bit is a count value (counting from 0 to 1) counting that the single cache line within the section of the memory is modified. A similar argument could be made for the cache counting value referencing Michael et al. However, as the sections only contain a single line the 'count values' don't truly tally up the number of lines as there can be no more than a single one.

Conclusion

33. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

34. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael Krofcheck whose telephone number is 571-272-8193. The examiner can normally be reached on Monday - Friday.

35. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

36. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Michael Krofcheck

MATTHEW KIM
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100